What is claimed is:

[Claim 1] 1. A electrostatic discharge (ESD) preventing-able level shifter, for receiving a first signal and outputting a second signal with a level corresponding to a level of the first signal, the first signal being transmitted between a first system voltage and a first ground voltage, and the second signal being transmitted between a second system voltage and a second ground voltage, the level shifter comprising:

an inverter, for receiving the first signal and outputting a first reverse signal, wherein the first reverse signal is reverse with respect to the first signal and is transmitted between the first system voltage and a first ground voltage;
a voltage converter, wherein a first input terminal of the voltage converter is adapted for receiving the first reverse signal, a second input terminal of the voltage converter is adapted for receiving the first signal and an output terminal of the voltage converter is adapted for outputting the second signal;
a first ESD clamp circuit, wherein a first terminal of the first ESD clamp circuit is coupled to the first input terminal of the voltage converter and a second terminal of the first ESD clamp circuit is coupled to the second ground voltage; and
a second ESD clamp circuit, wherein a first terminal of the second ESD clamp circuit is coupled to the second input terminal of the voltage converter and a second terminal of the second ESD clamp circuit is coupled to the second ground voltage.

[Claim 2] 2. The ESD preventing-able level shifter of claim 1, wherein the first ESD clamp circuit comprises an N-type transistor, wherein a drain of the N-type transistor is coupled to the first input terminal of the voltage converter, and wherein a gate, a source and a bulk of the N-type transistor are coupled to the second ground voltage.

[Claim 3] 3. The ESD preventing-able level shifter of claim 1, wherein the first ESD clamp circuit comprises a diode, wherein a cathode of the diode is coupled to the first input terminal of the voltage converter and an anode of the diode is coupled to the second ground voltage.

[Claim 4] 4. The ESD preventing-able level shifter of claim 1, wherein the inverter comprises:

a P-type transistor, wherein a source of the P-type transistor is coupled to the first system voltage, a gate of the P-type transistor is adapted for receiving the first signal, a drain of the P-type transistor is adapted for outputting the first reverse signal; and
an N-type transistor, wherein a gate of the N-type transistor is adapted for receiving the first signal, a drain of the N-type transistor is coupled to the drain of the P-type transistor, a source of the N-type transistor is coupled to the first ground voltage.

[Claim 5] 5. The ESD preventing-able level shifter of claim 1, wherein the voltage converter comprises:

a first transistor, wherein a first drain/source of the first transistor is coupled to the second system voltage;
a second transistor, wherein a gate of the second transistor is adapted for receiving the first reverse signal, a first source/drain of the second transistor is coupled to a second source/drain of the first transistor and a second source/drain terminal of the second transistor is coupled to the second ground voltage;
a third transistor, wherein a first source/drain of the third transistor is coupled to the second system voltage, a second source/drain of the third transistor is coupled to the gate of the first transistor and a gate of the third transistor is coupled to the second source/drain of the first transistor; and
a fourth transistor, wherein a gate of the fourth transistor is adapted for receiving a first signal, a first source/drain of the fourth transistor is coupled to the second source/drain of the third transistor and a second source/drain of the fourth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the fourth transistor is the second signal.

[Claim 6] 6. The ESD preventing-able level shifter of claim 5, wherein the first and third transistors are P-type transistors and the second and fourth transistors are N-type transistors.

[Claim 7] 7. The ESD preventing-able level shifter of claim 1, wherein the voltage converter comprises:

a first transistor, wherein a gate of the first transistor is adapted for receiving the first reverse signal and a first source/drain of the first transistor is coupled to the second system voltage;
a second transistor, wherein a gate of the second transistor is coupled to the gate of the first transistor and a first source/drain of the second transistor is coupled to a second source/drain of the first transistor;
a third transistor, wherein a first source/drain of the third transistor is coupled to a second source/drain of the second transistor and a second source/drain of the third transistor is coupled to the second ground voltage;
a fourth transistor, wherein a first source/drain of the fourth transistor is coupled to the second system voltage, a second source/drain of the fourth transistor is coupled to a gate of the third transistor and a gate of the fourth transistor is adapted for receiving the first signal;
a fifth transistor, wherein a gate of the fifth transistor is coupled to the gate of the fourth transistor and a first source/drain of the fifth transistor is coupled to the second source/drain of the fourth transistor; and
a sixth transistor, wherein a gate of the sixth transistor is coupled to the second source/drain of the first transistor, a first source/drain of the sixth transistor is coupled to a second source/drain of the fifth transistor and a second source/drain of the sixth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the fifth transistor is the second signal.

[Claim 8] 8. The ESD preventing-able level shifter of claim 7, wherein the first and fourth transistors are P-type transistors and the second, third, fifth and sixth transistors are N-type transistors.

[Claim 9] 9. A electrostatic discharge (ESD) preventing-able level shifter, for receiving a first signal and outputting a second signal with a level corresponding to a level of the first signal, the first signal being transmitted between a first system voltage and a first ground voltage, and the second signal being transmitted between a second

system voltage and a second ground voltage, the level shifter comprising:

an inverter, for receiving the first signal and outputting a first reverse signal, wherein the first reverse signal is reverse with respect to the first signal and is transmitted between the first system voltage and a first ground voltage;
a voltage converter, wherein a first input terminal of the voltage converter is adapted for receiving the first reverse signal, a second input terminal of the voltage converter is adapted for receiving the first signal and an output terminal of the voltage converter is adapted for outputting the second signal;
a first ESD clamp circuit, wherein a first terminal of the first ESD clamp circuit is coupled to the second system voltage and a second terminal of the first ESD clamp circuit is coupled to the first input terminal of the voltage converter; and
a second ESD clamp circuit, wherein a first terminal of the second ESD clamp circuit is coupled to the second system voltage and a second terminal of the second ESD clamp circuit is coupled to the second input terminal of the voltage converter.

[Claim 10] 10. The ESD preventing-able level shifter of claim 9, wherein the first ESD clamp circuit comprises an P-type transistor, a drain of the P-type transistor is coupled to the first input terminal of the voltage converter; and a gate, a source and a bulk of the P-type transistor are coupled to the second system voltage.

[Claim 11] 11. The ESD preventing-able level shifter of claim 9, wherein the first ESD clamp circuit comprises a diode, an anode of the diode is coupled to the first input terminal of the voltage converter and a cathode of the diode is coupled to the second system voltage.

[Claim 12] 12. The ESD preventing-able level shifter of claim 9, wherein the inverter comprises:

a P-type transistor, wherein a source of the P-type transistor is coupled to the first system voltage, a gate of the P-type transistor is adapted for receiving the first signal and a drain of the P-type transistor is adapted for outputting the first reverse signal; and

an N-type transistor, wherein a gate of the N-type transistor is adapted for receiving the first signal, a drain of the N-type transistor is coupled to the drain of the P-type transistor and a source of the N-type transistor is coupled to the first ground voltage.

[Claim 13] 13. The ESD preventing-able level shifter of claim 9, wherein the voltage converter comprises:

a first transistor, wherein a first source/drain of the first transistor is coupled to the second system voltage;
a second transistor, wherein a gate of the second transistor is adapted for receiving the first reverse signal and a first source/drain of the second transistor is coupled to a second source/drain of the first transistor;
a third transistor, wherein a gate of the third transistor is adapted for receiving the first reverse signal, a first source/drain of the third transistor is coupled to a second source/drain of the second transistor and a second source/drain of the third transistor is coupled to the second ground voltage;
a fourth transistor, wherein a first source/drain of the fourth transistor is coupled to the second system voltage, a gate of the fourth transistor is coupled to the second source/drain of the second transistor;
a fifth transistor, wherein a gate of the fifth transistor is adapted for receiving the first signal, a first source/drain of the fifth transistor is coupled to the second source/drain of the fourth transistor and a second source/drain of the fifth transistor is coupled to a gate of the first transistor; and
a sixth transistor, wherein a gate of the sixth transistor is adapted for receiving the first signal, a first source/drain of the sixth transistor is coupled to the second source/drain of the fifth transistor and a second source/drain of the sixth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the sixth transistor is the second signal.

[Claim 14] 14. The ESD preventing-able level shifter of claim 13, wherein the first, second, fourth and fifth transistors are P-type transistors, and third and sixth transistors are N-type transistors.

[Claim 15] 15. The ESD preventing-able level shifter of claim 9, wherein the voltage converter comprises:

a first transistor, wherein a first drain/source of the first transistor is coupled to the second system voltage and a gate of the first transistor is adapted for receiving the first reverse signal;
a second transistor, wherein a first source/drain of the second transistor is coupled to a second source/drain of the first transistor and a second source/drain terminal of the second transistor is coupled to the second ground voltage;
a third transistor, wherein a first source/drain of the third transistor is coupled to the second system voltage, a second source/drain voltage is coupled to the gate of the second transistor and a gate of the third transistor is adapted for receiving the first signal; and
a fourth transistor, wherein a gate of the fourth transistor is coupled to the second source/drain of the first transistor, a first source/drain of the fourth transistor is coupled to the second source/drain of the third transistor and a second source/drain of the fourth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the fourth transistor is the second signal.

[Claim 16] 16. The ESD preventing-able level shifter of claim 15, wherein the first and third transistors are P-type transistors, and the second and fourth transistors are N-type transistors.

[Claim 17] 17. The ESD preventing-able level shifter of claim 9, wherein the voltage converter comprises:

a first transistor, wherein a gate of the first transistor is adapted for receiving the first reverse signal and a first source/drain of the first transistor is coupled to the second system voltage;
a second transistor, wherein a gate of the second transistor is coupled to the gate of the first transistor and a first source/drain of the second transistor is coupled to a second source/drain of the first transistor;
a third transistor, wherein a first source/drain of the third transistor is coupled to a second source/drain of the second transistor and a second source/drain of the third transistor is coupled to the second ground voltage;

a fourth transistor, wherein a first source/drain of the fourth transistor is coupled to the second system voltage, a second source/drain of the fourth transistor is coupled to a gate of the third transistor and a gate of the fourth transistor is adapted for receiving the first signal;
a fifth transistor, wherein a gate of the fifth transistor is coupled to the gate of the fourth transistor and a first source/drain of the fifth transistor is coupled to the second source/drain of the fourth transistor; and
a sixth transistor, wherein a gate of the sixth transistor is coupled to the second source/drain of the first transistor, a first source/drain of the sixth transistor is coupled to a second source/drain of the fifth transistor and a second source/drain of the sixth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the fifth transistor is the second signal.

[Claim 18] 18. The ESD preventing-able level shifter of claim 17, wherein the first and fourth transistors are P-type transistors, and the second, third, fifth and sixth transistors are N-type transistors.

[Claim 19] 19. A electrostatic discharge (ESD) preventing-ablelevel shifter, for receiving a first signal and outputting a second signal with a level corresponding to a level of the first signal, the first signal being transmitted between a first system voltage and a first ground voltage and the second signal being transmitted between a second system voltage and a second ground voltage, the level shifter comprising:

an inverter, for receiving the first signal and outputting a first reverse signal, wherein the first reverse signal is reverse with respect to the first signal and is transmitted between the first system voltage and a first ground voltage;
a voltage converter, wherein a first input terminal of the voltage converter is adapted for receiving the first reverse signal, a second input terminal of the voltage converter is adapted for receiving the first signal and an output terminal of the voltage converter is adapted for outputting the second signal; and

an ESD clamp circuit, wherein a first terminal of the ESD clamp circuit is coupled to the second system voltage and a second terminal of the ESD clamp circuit is coupled to the first ground voltage.

[Claim 20] 20. The ESD preventing-able level shifter of claim 19, wherein the first ESD clamp circuit comprises a transistor, and wherein a collector of the transistor is coupled to the second system voltage, and an emitter and a base of the transistor are coupled to the first ground voltage.

[Claim 21] 21. The ESD preventing-able level shifter of claim 19, wherein the ESD clamp circuit comprises diode, wherein an anode of the diode is coupled to the first ground voltage and a cathode of the diode is coupled to the second system voltage.

[Claim 22] 22. The ESD preventing-able level shifter of claim 19, wherein the inverter comprises:

a P-type transistor, wherein a source of the P-type transistor is coupled to the first system voltage, a gate of the P-type transistor is adapted for receiving the first signal and a drain of the P-type transistor is adapted for outputting the first reverse signal; and
an N-type transistor, wherein a gate of the N-type transistor is adapted for receiving the first signal, a drain of the N-type transistor is coupled to the drain of the P-type transistor and a source of the N-type transistor is coupled to the first ground voltage.

[Claim 23] 23. The ESD preventing-able level shifter of claim 9, wherein the voltage converter comprises:

a first transistor, wherein a first source/drain of the first transistor is coupled to the second system voltage;
a second transistor, wherein a gate of the second transistor is adapted for receiving the first reverse signal and a first source/drain of the second transistor is coupled to a second source/drain of the first transistor;
a third transistor, wherein a gate of the third transistor is adapted for receiving the first reverse signal, a first source/drain of the third transistor is coupled to

a second source/drain of the second transistor and a second source/drain of the third transistor is coupled to the second ground voltage;
a fourth transistor, wherein a first source/drain of the fourth transistor is coupled to the second system voltage and a gate of the fourth transistor is coupled to the second source/drain of the second transistor;
a fifth transistor, wherein a gate of the fifth transistor is adapted for receiving the first signal, a first source/drain of the fifth transistor is coupled to the second source/drain of the fourth transistor and a second source/drain of the fifth transistor is coupled to a gate of the first transistor; and
a sixth transistor, wherein a gate of the sixth transistor is adapted for receiving the first signal, a first source/drain of the sixth transistor is coupled to the second source/drain of the fifth transistor and a second source/drain of the sixth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the sixth transistor is the second signal.

[Claim 24] 24. The ESD preventing-able level shifter of claim 23, wherein the first, second, fourth and fifth transistors are P-type transistors and the third and sixth transistors are N-type transistors.